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A pulse interrupt is a variant of an edge model. You must ensure that the pulse is sampled on the rising edge of the Cortex-M4 clock, FCLK, instead of being

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asynchronous. For level interrupts, if the signal is not deasserted before the return from the interrupt routine, the interrupt again enters the pending state and re-activates.

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The Cortex-M4 processor is a low-
power processor that features low
gate count, low interrupt latency,

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Documentation – Arm Developer Processor Refers to the Cortex-M4 processor, as supplied by ARM. Device Refers to an

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Cortex-M4 Devices - ARM

The Cortex-M4F processor is a Cortex-M4 processor that includes the optional FPU. In this chapter, the generic term processor means only the Cortex-M4F processor.

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Manual. A mechanism that indicates to a core that the attempted memory access is invalid or not allowed or that the data returned by the memory access is invalid. An abort can be caused ...

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Manual: Glossary

In this manual, in general: † any reference to the processor applies to either the Cortex-M4 processor or the Cortex-M4F processor, as appropriate † any reference to the Cortex-M4 processor applies also to the Cortex-M4F processor, as

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appropriate. The context makes it clear if information applies to only one of the processor options.

CoreSight ETM -M4 - ARM

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M23, Cortex-M33, Cortex-M35P,
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